The bandwidth will be dictated by the low-pass filter formed by the output impedance of the stage and the load capacitance. A pole will be formed at

$$f_3 = 1/(2\pi R_L C_L) = 0.159/(5\ \text{k}\Omega * 100\ \text{pF}) = 318\ \text{kHz}$$

As an approximation, the collector-base capacitance should also be considered part of C_L. The bandwidth of a CE stage is often further limited by the collector-base capacitance of the transistor when the CE stage is fed from a source with significant impedance. The source must supply current to charge and discharge the collector-base capacitance through the large voltage excursion that exists between the collector and the base. This phenomenon is called the *Miller effect*.

Suppose the collector-base capacitance is 5 pF and assume that the CE stage is being fed from a 5-kΩ source impedance R_S. Recall that the voltage gain G of the circuit in Figure 2.5a was approximately 192. This means that the voltage across C_{cb} is 193 times as large as the input signal (bearing in mind that the input signal is out of phase with the output signal, adding to the difference). This means that the current flowing through C_{cb} is 193 times as large as the current that would flow through it if it were connected from the base to ground instead of base to collector. The input circuit thus sees an effective input capacitance C_{in} that is $1 + G$ times that of the collector-base capacitance. This phenomenon is referred to as *Miller multiplication* of the capacitance. In this case the effective value of C_{in} would be 965 pF.

The base-collector capacitance effectively forms a shunt feedback circuit that ultimately controls the gain of the stage at higher frequencies where the reactance of the capacitor becomes small. As frequency increases, a higher proportion of the input signal current must flow to the collector-base capacitance as opposed to the small fixed amount of signal current required to flow into the base of the transistor. If essentially all of the input signal current flowed through the collector-base capacitance, the gain of the stage would simply be the ratio of the capacitive reactance of C_{cb} to the source resistance

$$G = \frac{X_{Ccb}}{R_S} = \frac{1}{(2\pi f C_{cb})(R_S)} = \frac{0.159}{(f C_{cb} R_S)}$$

This represents a value of gain that declines at 6 dB per octave as frequency increases. This decline will begin at a frequency where the gain calculated here is equal to the low-frequency gain of the stage. The Miller effect is often used to advantage in providing the high-frequency roll-off needed to stabilize a negative feedback loop. This is referred to as *Miller compensation*.

Differential Amplifier

The differential amplifier is illustrated in Figure 2.6. It is much like a pair of common emitter amplifiers tied together at the emitters and biased with a common current. This current is called the *tail current*. The arrangement is often referred to as a *long-tailed pair* (*LTP*).

The differential amplifier routes its tail current to the two collectors of Q1 and Q2 in accordance with the voltage differential across the bases of Q1 and Q2. If the base voltages are equal, then equal currents will flow in the collectors of Q1 and Q2. If the base of Q1 is more positive than that of Q2, more of the tail current will flow in the collector of Q1 and less will flow in the collector of Q2. This will result in a larger voltage drop across the collector load resistor R_{L1} and a smaller voltage drop across load resistor R_{L2}.

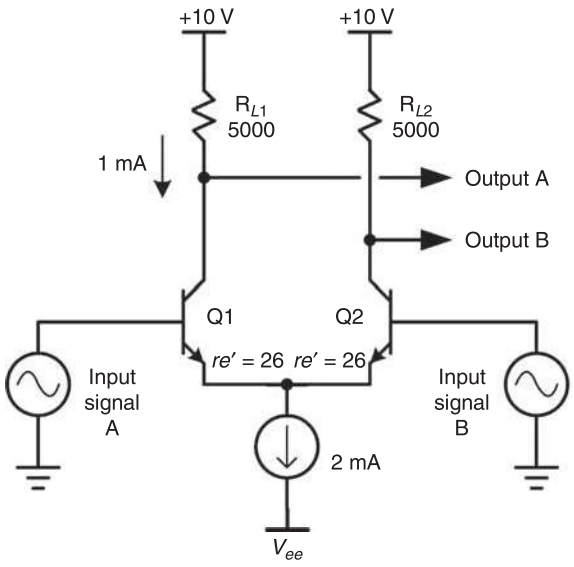

Figure 2.6 Differential amplifier.

Output A is thus inverted with respect to Input A, while Output B is noninverted with respect to Input A.

Visualize the intrinsic emitter resistance *re′* present in each emitter leg of Q1 and Q2. Recall that the value of *re′* is approximately 26 Ω divided by the transistor operating current in milliamperes. With 1 mA flowing nominally through each of Q1 and Q2, each can be seen as having an emitter resistance *re′* of 26 Ω. Note that since $gm = 1/re'$ is dependent on the instantaneous transistor current, the values of *gm* and *re′* are somewhat signal dependent, and indeed this represents a nonlinearity that gives rise to distortion.

Having visualized the ideal transistor with emitter resistance *re′*, one can now assume that the idealized internal emitter of each device moves exactly with the base of the transistor, but with a fixed DC voltage offset equal to V_{be}. Now look what happens if the base of Q1 is 5.2 mV more positive than the base of Q2. The total emitter resistance separating these two voltage points is 52 Ω, so a current of 5.2 mV/52 Ω = 0.1 mA will flow from the emitter of Q1 to the emitter of Q2. This means that the collector current of Q1 will be 100 μA more than nominal, and the collector current of Q2 will be 100 μA less than nominal. The collector currents of Q1 and Q2 are thus 1.1 mA and 0.9 mA, respectively, since they must sum to the tail current of 2.0 mA (assuming very high β for the transistors).

This 100-μA increase in the collector current of Q1 will result in a change of 500 mV at Output A, due to the collector load resistance of 5000 Ω. A 5.2-mV input change at the base of Q1 has thus caused a 500-mV change at the collector of Q1, so the stage gain to Output A in this case is approximately 500/5.2 = 96.2. More significantly, the stage gain defined this way is just equal numerically to the load resistance of 5000 Ω divided by the total emitter resistance *re′* = 52 Ω across the emitters.

Had additional external emitter degeneration resistors been included in series with each emitter, their value would have been added into this calculation. For example, if 48-Ω emitter degeneration resistors were employed, the gain would then become 5000/(52 + 48 + 48 + 52) = 5000/200 = 25. This approach to estimating stage gain is a very

important back-of-the-envelope concept in amplifier design. In a typical amplifier design, one will often start with these approximations and then knowingly account for some of the deviations from the ideal. This will be evident in the numerous design analyses to follow.

It was pointed out earlier that the change in transconductance of the transistor as a function of signal current can be a source of distortion. Consider the situation where a negative input signal at the base of Q1 causes Q1 to conduct 0.5 mA and Q2 to conduct 1.5 mA. The emitter resistance *re′* of Q1 is now 26/0.5 = 52 Ω. The emitter resistance *re′* of Q2 is now 26/1.5 = 17.3 Ω. The total emitter resistance from emitter to emitter has now risen from 52 Ω in the case above to 69.3 Ω. This results in a reduced gain of 5000/69.3 = 72.15. This represents a reduction in gain by a factor of 0.75, or about 25%. This is an important origin of distortion in the LTP. The presumed signal swing that caused the imbalance of collector currents between Q1 and Q2 resulted in a substantial decrease in the incremental gain of the stage. More often than not, distortion is indeed the result of a change in incremental gain as a function of instantaneous signal amplitude.

The gain of an LTP is typically highest in its balanced state and decreases as the signal goes positive or negative away from the balance point. This symmetrical behavior is in contrast to the asymmetrical behavior of the common-emitter stage, where the gain increases with signal swing in one direction and decreases with signal swing in the other direction. To first order, the symmetrical distortion here is third harmonic distortion, while that of the CE stage is predominantly second harmonic distortion.

Notice that the differential input voltage needed to cause the above imbalance in the LTP is only on the order of 25 mV. This means that it is fairly easy to overload an LTP that does not incorporate emitter degeneration. This is of great importance in the design of most power amplifiers that employ an LTP input stage.

Suppose the LTP is pushed to 90% of its output capability. In this case Q1 would be conducting 0.1 mA and Q2 would be conducting 1.9 mA. The two values of *re′* will be 260 Ω and 14 Ω, for a total of 274 Ω. The gain of the stage is now reduced to 5000/274 = 18.25. The nominal gain of this un-degenerated LTP was about 96.2. The incremental gain under these large signal conditions is down by about 80%, implying gross distortion.

As in the case of the CE stage, adding emitter degeneration to the LTP will substantially reduce its distortion while also reducing its gain. In summary we have the approximation

$$\text{Gain} = \frac{R_{L1}}{2(r_e' + R_e)}$$

where R_{L1} is a single-ended collector load resistance and R_e is the value of external emitter degeneration resistance in each emitter of the differential pair. This gain is for the case where only a single-ended output is taken from the collector of Q1. If a differential output is taken from across the collectors of Q1 and Q2, the gain will be doubled. For convenience, the total emitter-to-emitter resistance in an LTP, including the intrinsic *re′* resistances, will be called R_{LTP}. In the example above,

$$R_{LTP} = 2(re' + R_e)$$

Emitter Follower

The emitter follower (*EF*) is essentially a unity voltage gain amplifier that provides current gain. It is most often used as a buffer stage, permitting the high impedance output of a CE or LTP stage to drive a heavier load.

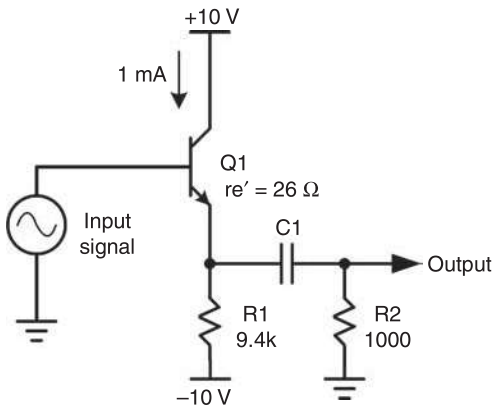

FIGURE 2.7 Emitter follower.

The emitter follower is illustrated in Figure 2.7. It is also called a common collector (*CC*) stage because the collector is connected to an AC ground. The output pulldown resistor R1 establishes a fairly constant operating collector current in Q1. For illustration, a load resistor R2 is being driven through a coupling capacitor. For AC signals, the net load resistance R_L at the emitter of Q1 is the parallel combination of R1 and R2. If *re′* of Q1 is small compared to R_L, virtually all of the signal voltage applied to the base of Q1 will appear at the emitter, and the voltage gain of the emitter follower will be nearly unity.

The signal current in the emitter will be equal to V_{out}/R_L, while the signal current in the base of Q1 will be this amount divided by the β of the transistor. It is immediately apparent that the input impedance seen looking into the base of Q1 is equal to the impedance of the load multiplied by the current gain of Q1. This is the most important function of the emitter follower.

As mentioned above, the voltage gain of the emitter follower is nearly unity. Suppose R1 is 9.4 kΩ and the transistor bias current is 1 mA. The intrinsic emitter resistance *re′* will then be about 26 Ω. Suppose R2 is 1 kΩ, making net R_L equal to 904 Ω. The voltage gain of the emitter follower is then approximately

$$G = R_L/(R_L + re') = 0.97$$

At larger voltage swings the instantaneous collector current of Q1 will change with signal, causing a change in *re′*. This will result in a change in incremental gain that corresponds to distortion. Suppose the signal current in the emitter is 0.9 mA peak in each direction, resulting in an output voltage of about 814 mV peak. At the negative peak swing, emitter current is only 0.1 mA and *re′* has risen to 260 Ω. Incremental gain is down to about 0.78. At the positive peak swing the emitter current is 1.9 mA and *re′* has fallen to 13.7 Ω; this results in a voltage gain of 0.985.

Voltage gain has thus changed by about 21% over the voltage swing excursion; this causes considerable second harmonic distortion. One solution to this is to reduce R1 so that a greater amount of bias current flows, making *re′* a smaller part of the gain equation. This of course also reduces net R_L somewhat. A better solution is to replace R1 with a constant current source.

The transformation of low-value load impedance to much higher input impedance by the emitter follower is a function of the current gain of the transistor. The β is

a function of frequency, as dictated by the f_T of the transistor. This means, for example, that a resistive load will be transformed to impedance at the input of the emitter follower that eventually begins to decrease with frequency as β_{AC} decreases with frequency. A transistor with a nominal β of 100 and f_T of 100 MHz will have an f_β of 1 MHz. The AC β of the transistor will begin to drop at 1 MHz. The decreasing input impedance of the emitter follower thus looks capacitive in nature, and the phase of the input current will lead the phase of the voltage by an amount approaching 90 degrees.

The impedance transformation works both ways. Suppose we have an emitter follower that is driven by a source impedance of 1 kΩ. The low-frequency output impedance of the EF will then be approximately 1 kΩ divided by β, or about 10 Ω (ignoring *re*′). However, the output impedance will begin to rise above 1 MHz where β begins to fall. Impedance that increases with frequency is inductive. Thus, Z_{out} of an emitter follower tends to be inductive at high frequencies.

Now consider an emitter follower that is loaded by a capacitance. This can lead to instability, as we will see. The load impedance presented by the capacitance falls with increasing frequency. The amount by which this load impedance is multiplied by β_{AC} also falls with frequencies above 1 MHz. This means that the input impedance of the emitter follower is ultimately falling with the square of frequency. It also means that the current in the load, already leading the voltage by 90 degrees, will be further transformed by another 90 degrees by the falling transistor current gain with frequency. This means that the input current of the emitter follower will lead the voltage by an amount approaching 180 degrees. When current is 180 degrees out of phase with voltage, this corresponds to a *negative resistance*. This can lead to instability, since the input impedance of this emitter follower is a frequency-dependent negative resistance under these conditions. This explains why placing a resistance in series with the base of an emitter follower will sometimes stabilize it; the positive resistance adds to the negative resistance by an amount that is sufficient to make the net resistance positive.

There is one more aspect of emitter follower behavior that pertains largely to its use in the output stage of a power amplifier. It was implied above that if an emitter follower was driven from a very low impedance source that its output impedance would simply be *re*′ of its transistor. This is not quite the whole story. Transistors have finite base resistance. The output impedance of an emitter follower will actually be the value of *re*′ plus the value of the base resistance divided by β of the transistor. This can be significant in an output stage. Consider a power transistor operating at 100 mA. Its *re*′ will be about 0.26 Ω. Suppose that transistor has a base resistance of 5 Ω and a current gain of 50. The value of the transformed base resistance will be 0.1 Ω. This is not insignificant compared to the value of *re*′ and must be taken into account in some aspects of design. This can also be said for the emitter resistance of the power transistor, which may range from 0.01 to 0.1 Ω.

The simplicity of the emitter follower, combined with its great ability to buffer a load, accounts for it being the most common type of circuit used for the output stage of power amplifiers. An emitter follower will often be used to drive a second emitter follower to achieve even larger amounts of current gain and buffering. This arrangement is sometimes called a *Darlington connection*. Such a pair of transistors, each with a current gain of 50, can increase the impedance seen driving a load by a factor of 2500. Such an output stage driving an 8-Ω load would present an input impedance of 20,000 Ω.

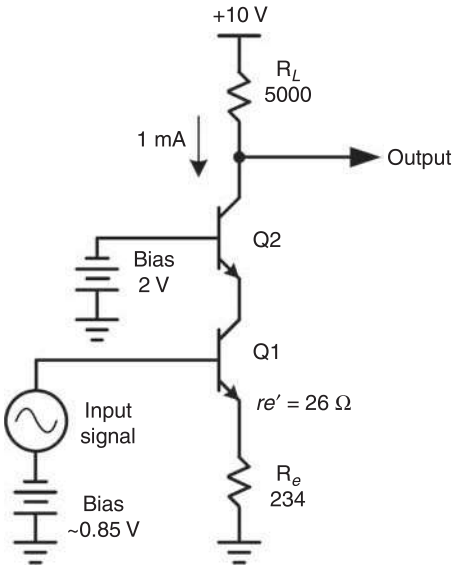

FIGURE 2.8 Cascode.

Cascode

A cascode stage is implemented by Q2 in Figure 2.8. The cascode stage is also called a *common base* stage because the base of its transistor is connected to AC ground. Here the cascode is being driven at its emitter by a CE stage comprising Q1. The most important function of a cascode stage is to provide isolation. It provides near-unity current gain, but can provide very substantial voltage gain. In some ways it is like the dual of an emitter follower.

A key benefit of the cascode stage is that it largely keeps the collector of the driving CE stage at a constant potential. It thus isolates the collector of the CE stage from the large swing of the output signal. This eliminates most of the effect of the collector-base capacitance of Q2, resulting in wider bandwidth due to suppression of the Miller effect. Similarly, it mitigates distortion caused by the nonlinear collector-base junction capacitance of the CE stage, since very little voltage swing now appears across the collector-base junction to modulate its capacitance.

The cascode connection also avoids most of the Early effect in the CE stage by nearly eliminating signal swing at its collector. A small amount of Early effect remains, however, because the signal swing at the base of the CE stage modulates the collector-base voltage slightly.

If the current gain of the cascode transistor is 100, then 99% of the signal current entering the emitter will flow in the collector. The input-output current gain is thus 0.99. This current transfer factor from emitter to collector is sometimes referred to as the *alpha* of the transistor.

The Early effect resistance *ro* still exists in the cascode transistor. It is represented as a resistance *ro* connected from collector to emitter. Suppose *ro* is only 10 kΩ. Is the output impedance of the collector of the cascode 10 kΩ? No, it is not.

Recall that 99% of the signal current entering the emitter of the cascode re-appears at the collector. This means that 99% of the current flowing in *ro* also returns to the

collector. Only the lost 1% of the current in *ro* results in a change in the net collector current at the collector terminal. This means that the net effect of *ro* on the collector output impedance in the cascode is roughly like that of a 1-MΩ resistor to ground. This is why the output impedance of cascode stages is so high even though Early effect still is present in the cascode transistor.

$$R_{out} = \beta * ro$$

$$ro = \frac{VA + V_{ce}}{I_c}$$

$$ro \approx VA/I_c \qquad \text{at low } V_{ce}$$

$$R_{out} = \beta * VA/I_c$$

Notice that the product of β and *VA* is the Early effect figure of merit mentioned previously. The output resistance of a cascode is thus the FOM divided by the collector current.

$$R_{out} = \text{FOM}/I_c$$

Current Mirror

Figure 2.9a depicts a very useful circuit called a current mirror. If a given amount of current is sourced into Q1, that same amount of current will be sunk by Q2, assuming that the emitter degeneration resistors R1 and R2 are equal, that the transistor V_{be} drops are the same, and that losses through base currents can be ignored. The values of R1 and R2 will often be selected to drop about 100 mV to ensure decent matching in the face of unmatched transistor V_{be} drops, but this is not critical.

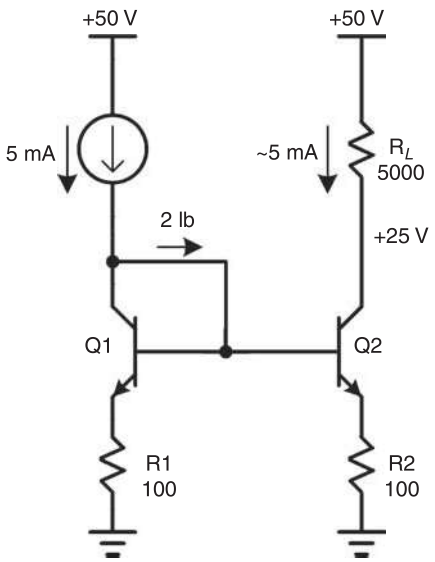

Figure 2.9a Simple current mirror.

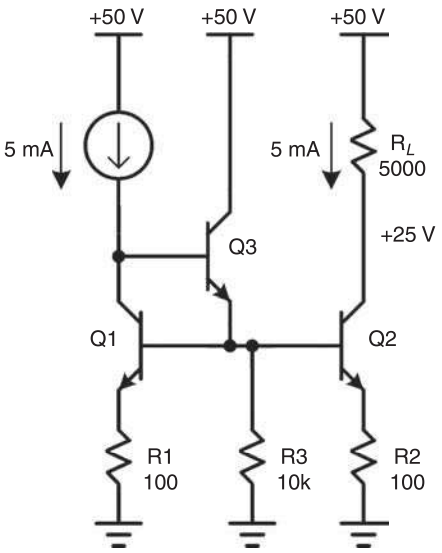

Figure 2.9b Improved current mirror.

If R1 and R2 are made different, a larger or smaller multiple if the input current can be made to flow in the collector of Q2. In practice, the base currents of Q1 and Q2 cause a small error in the output current with respect to the input current. In the example above, if transistor β is 100, the base current I_b of each transistor will be 50 μA, causing a total error of 100 μA, or 2% in the output current.

Figure 2.9b shows a variation of the current mirror that minimizes errors due to the finite current gain of the transistors. Here emitter follower Q3, often called a *helper* transistor, provides current gain to minimize that error. Resistor R3 assures that a small minimum amount of current flows in Q3 even if the current gains of Q1 and Q2 are very high. Note that the input node of the current mirror now sits one V_{be} higher above the supply rail than in Figure 2.9a.

Many other variations of current mirrors exist, such as the *Wilson* current mirror shown in Figure 2.9c. The Wilson current mirror includes transistors Q1, Q2, and Q3. Input current is applied to the base of Q3 and is largely balanced by current flowing in the collector of Q1. Input current that flows into the base of output transistor Q3 will turn Q3 on, with its emitter current flowing through Q2 and R2. Q1 and Q2 form a conventional current mirror. The emitter current of Q3 is mirrored and pulled from the source of input current by Q1.

Any difference between the current of Q1 and the input current is available to drive the base of Q3. If the input current exceeds the mirrored emitter current of Q3, the base voltage of Q3 will increase, causing the emitter current of Q3 to increase and self-correct the situation with feedback action. The equilibrium condition can be seen to be when the input current and the output current are the same, providing an overall 1:1 current mirror function.

Notice that in normal operation all three of the transistors operate at essentially the same current, namely the supplied input current. Ignoring the Early effect, all of the base currents will be the same if the betas are matched. Assume that each base current

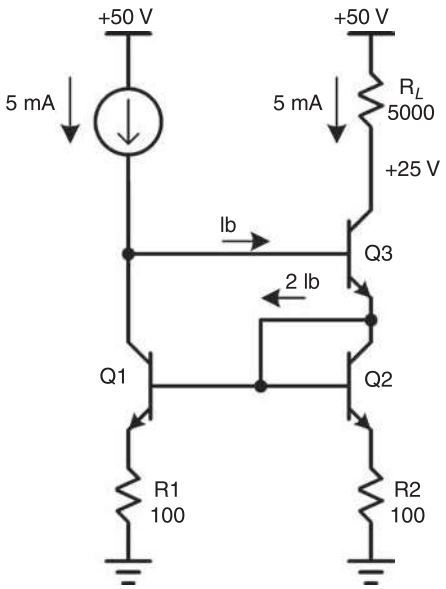

Figure 2.9c Wilson current mirror.

is I_b and that the collector current in Q1 is equal to I. It can be quickly seen that the input current must then be $I + I_b$ and that the emitter current of Q3 must be $I + 2I_b$. It is then evident that the collector current of Q3, which is the output current, will be $I + I_b$, which is the same as the input current. This illustrates the precision of the input-output relationship when the transistors are matched.

Transistor Q3 acts much like a cascode, and this helps the Wilson current mirror to achieve high output impedance. Transistors Q1 and Q2 operate at a low collector voltage, while output transistor Q3 will normally operate at a higher collector voltage. Thus, the Early effect will cause the base current of Q3 to be smaller, and this will result in a slightly higher voltage-dependent output current. This is reflected in the output resistance of the Wilson current mirror.

Current Sources

Current sources are used in many different ways in a power amplifier, and there are many different ways to make a current source. The distinguishing feature of a current source is that it is an element through which a current flows wherein that current is independent of the voltage across that element. The current source in the tail of the differential pair is a good example of its use.

Most current sources are based on the observation that if a known voltage is impressed across a resistor, a known current will flow. A simple current source is shown in Figure 2.10a. The voltage divider composed of R2 and R3 places 2.7 V at the base of Q1. After a V_{be} drop of 0.7 V, about 2 V is impressed across emitter resistor R1. If R1 is a 400-Ω resistor, 5 mA will flow in R1 and very nearly 5 mA will flow in the collector of Q1. The collector current of Q1 will be largely independent of the voltage at the collector of Q1, so the circuit behaves as a decent current source. The load resistance R_L is just shown for purposes of illustration. The output impedance of the current source itself (not including the shunting effect of R_L) will be determined largely by the Early effect in

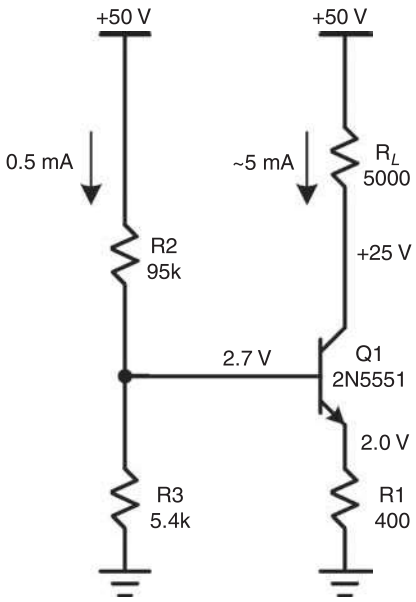

Figure 2.10a Simple current source.

the same way as for the CE stage. The output impedance for this current source is found by SPICE simulation to be about 290 kΩ.

In Figure 2.10b, R3 is replaced with a pair of silicon diodes. Here one diode drop is impressed across R1 to generate the desired current. The circuit employs 1N4148 diodes biased with the same 0.5 mA used in the voltage divider in the first example. Together

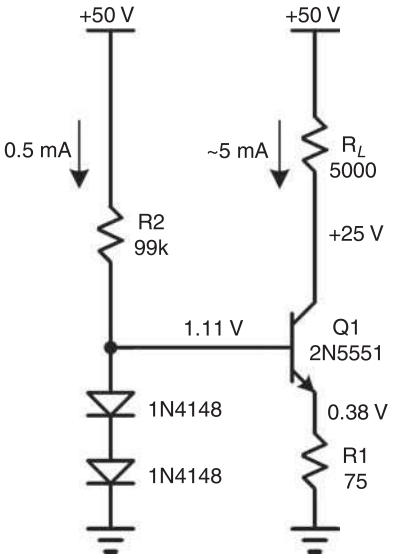

Figure 2.10b Current source using diodes.

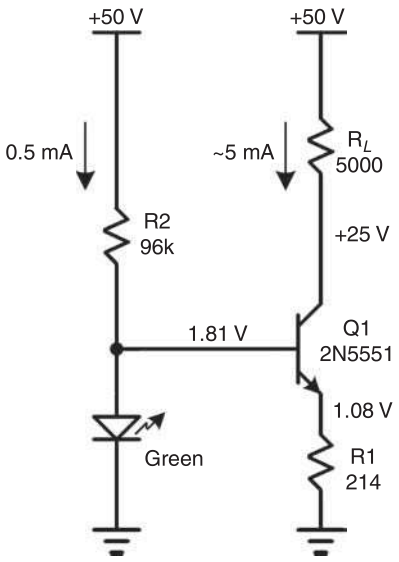

Figure 2.10c Current source using LED.

they drop only about 1.1 V, and about 0.38 V is impressed across the 75-Ω resistor R1. The output impedance of this current source is approximately 300 kΩ, about the same as the one above.

Turning to Figure 2.10c, R3 is replaced instead with a Green LED, providing a convenient voltage reference of about 1.8 V, putting about 1.1 V across R1. Once again, 0.5 mA is used to bias the LED. The output impedance of this current source is about 750 kΩ. It is higher than in the design of Figure 2.10b because there is effectively more emitter degeneration for Q1 with the larger value of R1.

R3 is replaced with a 6.2-V *Zener* diode in Figure 2.10d. This puts about 5.5 V across R1. The output impedance of this current source is about 2 MΩ, quite a bit higher than the earlier arrangements due to the larger emitter degeneration for Q1. The price paid here is that the base of the transistor is fully 6.2 V above the supply rail, reducing headroom in some applications.

In Figure 2.10e, a current mirror fed from a known supply voltage is used to implement a current source. Here a 1:1 current mirror is used and 5 mA is supplied from the known power rail. The output impedance of this current source is about 230 kΩ. Only 0.25 V is dropped across R1 (corresponding to 10:1 emitter degeneration), and the base is only 1 V above the rail.

Figure 2.10f illustrates a clever two-transistor feedback circuit that is used to force one V_{be} of voltage drop across R1. It does so by using transistor Q2 to effectively regulate the current of Q1. If the current of Q1 is too large, Q2 will be turned on harder and pull down on the base of Q1, adjusting its current downward appropriately. As in Figure 2.10a through 2.10d, a 0.5-mA current is supplied to bias the current source. This current flows through Q2. The output impedance of this current source is an impressive 3 MΩ. This circuit achieves higher output impedance than the Zener-based version and yet only requires the base of Q1 to be 1.4 V above the power rail. This circuit can also be used to place an overcurrent limit on a CE transistor stage implemented with Q1.

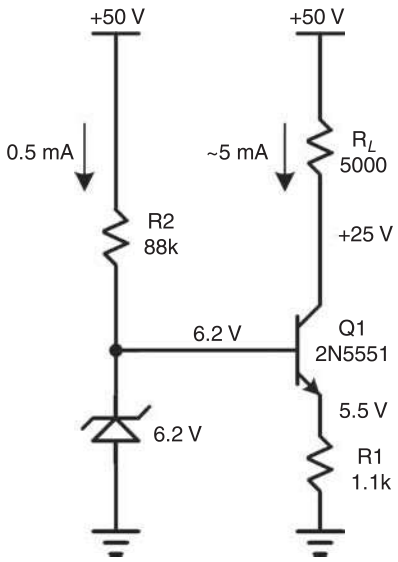

Figure 2.10d Current source using Zener diode.

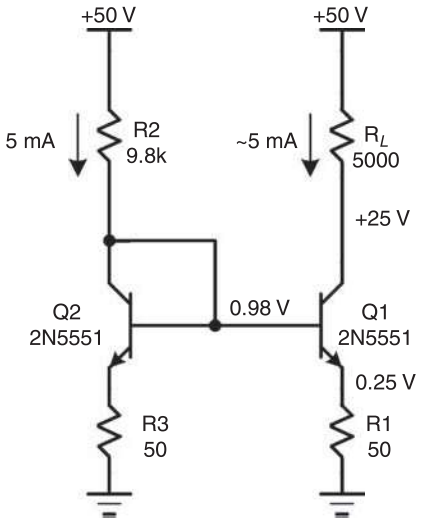

Figure 2.10e Current mirror current source.

This circuit will work satisfactorily even if less than 0.5 mA (one-tenth of the output current) is supplied as bias for Q2, but then the output impedance will fall to a lower value and the "quality" of the current source will suffer somewhat. This happens because at lower collector current, Q2 has less transconductance and its feedback control of the current variations in Q1 as a result of the Early effect is less strong. If the bias current is reduced to 0.1 mA, for example, the output impedance falls to about 1 MΩ.

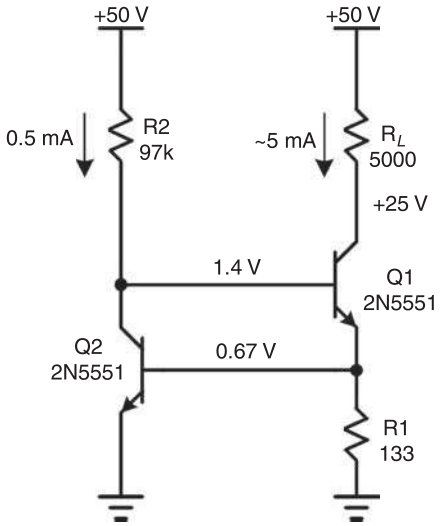

FIGURE 2.10f Feedback current source.

V_{be} Multiplier

Figure 2.11 shows what is called a V_{be} *multiplier*. This circuit is used when a voltage drop equal to some multiple of V_{be} drops is needed. This circuit is most often used as the bias spreader for power amplifier output stages, partly because its voltage is conveniently adjustable.

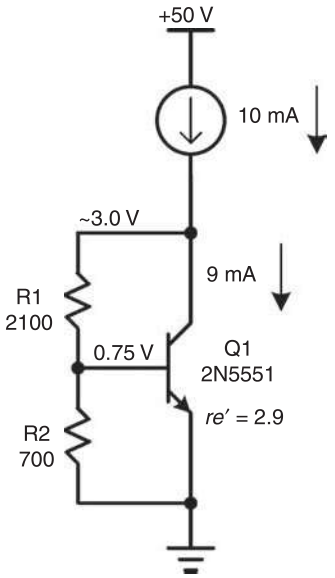

FIGURE 2.11 V_{be} multiplier.