its effectiveness is sometimes temperature dependent as a result of transistor beta temperature dependence. The correction current can be injected on either side of the input through a large-value resistor.

#### **JFET Input Stages**

Although JFET input stages typically start off with greater input voltage offset than BJT stages (assuming both are dual matched pairs), it should be very apparent by now that their absence of input bias current makes them superior in terms of overall amplifier DC offset. They free the designer from trying to balance the DC resistances on the input and feedback sides of the input stage.

### 8.2 DC Servo Basics

The concept of a DC servo is quite simple. The average DC level at the output is extracted by a low-pass filter, amplified and fed back to the feedback side of the input stage. This drives the output DC value to zero or a very small value. This permits the use of a low-impedance DC-coupled feedback network while retaining high amplifier input impedance. In practice, an integrator is almost always used to provide both the low-pass filtering function and the gain. This is illustrated in Figure 8.5 where the input pair of the amplifier is implemented with JFETs. Without the DC servo, output offset would be 200 mV with a JFET offset of 10 mV.

The amplifier output is applied to a conventional inverting integrator followed by a unity-gain inverter to provide the proper feedback polarity. The integrator input

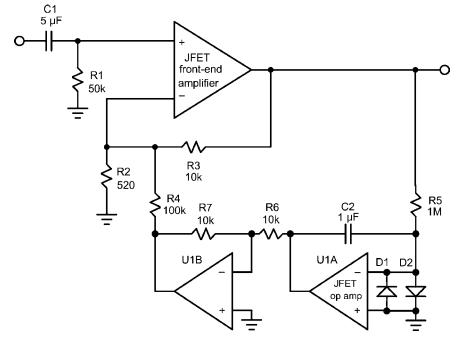


FIGURE 8.5 A power amplifier with a simple DC servo using an inverting integrator.

resistor R5 is chosen to be 1  $M\Omega$ , while the integrator capacitor C2 is set to 1  $\mu$ F. The integrator is usually implemented with a JFET op amp to avoid integrator offsets created by input bias current. The integrator inputs are protected from excessive input voltages by diodes D1 and D2. The servo output from the inverter is applied to the feedback input of the amplifier input stage. This effectively creates an auxiliary feedback loop that is active at DC and very low frequencies.

If there exists a small positive average DC value at the amplifier output, integrator capacitor C2 will charge by the current sourced to it through R5, driving the output of the integrator negative. The output of the inverter will go positive and source current to the feedback input to drive the feedback input positive. This in turn will drive the output of the amplifier negative. The very high DC gain of the integrator forces the output of the amplifier to essentially zero. In practice, it forces the output voltage to equal the input offset voltage of the integrator op amp in the absence of input bias current. This will typically be less than  $\pm 10$  mV for a JFET op amp.

On paper the complexity of the amplifier is higher, but cost and space for the same quality is lower. The only major components are a dual op amp and a film integrating capacitor. The output of the servo drives the amplifier's feedback input node through a fairly high-value resistor (R4) because it needs only to inject enough correction current to overcome the maximum anticipated input-referred offset error. The large resistor tends to reduce the ability of the servo and its op amp to adversely impact sound quality via noise or distortion in the servo. As discussed below, caution is required to avoid setting R4 too high.

The servo provides increased negative feedback as frequency goes lower. As such it does indeed introduce a high-pass filter function into the audio path, but so did the simple electrolytic in the feedback return leg. With the DC servo, however, you have now removed an evil 100- $\mu$ F electrolytic that would have been bad for the sound even if bypassed by a smaller film capacitor.

#### **DC Servo Architectures**

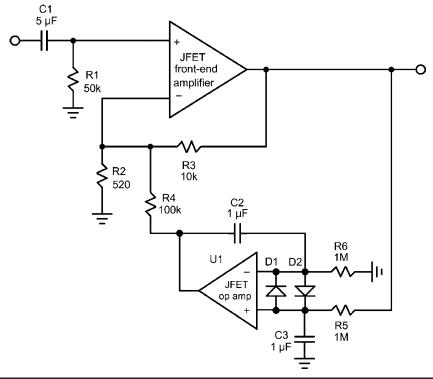
Figure 8.6 shows a noninverting integrator that requires only one op amp. It is like a single op-amp differential amplifier but with the feedback and shunt resistors replaced with capacitors to make it into an integrator. It requires two capacitors, and this is a disadvantage.

I prefer DC servos that employ a dual op amp and only require a single integrating capacitor, perhaps on the order of 1  $\mu$ F. It is quite economical to employ a high-quality 1- $\mu$ F film capacitor. Dual op amps that are of high quality are also relatively inexpensive.

#### Setting the Low-Frequency Corner

Now let's set the LF 3-dB point for the overall amplifier to 1 Hz, excluding the high-pass filter formed by the input coupling capacitor. This means that the gain around the servo loop will fall to unity at 1 Hz. This also means that the amount of feedback provided through the servo circuit equals that provided through the feedback network at 1 Hz.

Assume that the feedback network consists of a series  $10\text{-k}\Omega$  feedback resistor with a  $520\text{-}\Omega$  shunt resistor, setting the amplifier closed-loop gain at 20. The attenuation of the feedback network is 20:1. The servo circuit should provide this same amount of attenuation at 1 Hz. Set the integrator resistor to 160 k $\Omega$  and the integrator capacitor to  $1\,\mu\text{F}$ . This makes the gain of the integrator unity at 1 Hz. Make the inverter gain unity. Set the servo signal injection resistor to 10 k $\Omega$ . This combination of component values



**Figure 8.6** A DC servo implemented with a noninverting integrator requiring only one op amp but two integrator capacitors.

makes the servo feedback signal equal to the main feedback signal at 1 Hz. The gain of the servo to the output of the inverter is only 0.1 at 10 Hz. This means that a 40-V-peak, 10-Hz test signal at the output of the amplifier will produce 4-V peak at the output of the servo op amps. They will have adequate margin against clipping if they are powered from  $\pm 15$ -V supplies.

#### **Amount of Offset to Be Corrected**

If a DC servo is used with a low-impedance DC-coupled feedback network, then the DC servo must correct the full amount of offset created by input bias current flowing in the input return resistor. In the case above where a single NPN differential pair is used with transistors biased at 1 mA and an input return resistance of 50 k $\Omega$ , the DC servo must be able to create a full 0.5 V of compensating offset on the feedback side of the LTP. This assumes that beta of the input transistors is 100.

This amount of compensating offset is substantial. This offset needs to be taken into account in determining how much correction range the servo will need to be able to apply. In the example cited above, if the op amp can provide  $\pm 14$  V, the servo will be able to accommodate  $\pm 0.7$  V of input offset. Other DC servo designs that employ a larger servo injection resistance (sometimes for good reason) may not be able to satisfy the  $\pm 0.5$ -V requirement. Here, there is an advantage in using JFETs for the LTP because the input offset due to base current is eliminated.

An interesting trick shown in Figure 8.3b is to add a DC balancing resistor between the feedback shunt resistor and the input of the BJT input stage. The value of this resistor is chosen to be that of the return resistor less the DC resistance of the feedback network. The added resistance will equalize the offset due to input bias current. This resistor can be bypassed with a  $1-\mu F$  film capacitor, since signal current flow in it is very small. This will reduce the required DC servo control range when BJT input stages are used.

#### **Servo Control Range**

My philosophy in applying a DC servo is that it should do as little as possible to the amplifier circuit, and its effect should be as subtle as possible. The DC servo is there to eliminate the *natural* offset of the amplifier that would exist if a capacitor in the feedback return leg were not used. The servo should not be more powerful than is necessary to do this job with some margin. This philosophy argues for the use of a servo injection resistor with the highest value that is consistent with meeting all servo performance requirements.

#### **Servo Clipping**

The signal voltage at the output of the DC servo will increase as frequency decreases. If the amplifier is subjected to full-power subsonic signals during testing, it is possible that the output of the DC servo will clip. For this reason, the gain of the DC servo at low frequencies must be kept in mind. If that gain is set too high so as to allow a larger value of injection resistor, then the clipping point might be reached at uncomfortably high frequencies. The tendency to clip is also governed by the chosen low-frequency cutoff frequency for which the servo is designed. Servos designed to yield a higher cutoff frequency will tend to clip at a higher frequency. A good rule of thumb is that the servo should never clip at a frequency higher than 10 Hz when the amplifier is operating at full power.

The DC servo described above having a 1-Hz bandwidth will produce a peak signal swing of 4-V peak when the amplifier is producing 40-V peak at 10 Hz (corresponding to 100 W/8  $\Omega$ ). A 400-W/8- $\Omega$  amplifier will only produce an 8-V peak output from the servo at 10 Hz, indicating that this servo design is adequate for such an amplifier, but there is a caveat.

### **Servo Headroom**

If the servo op amp can produce  $\pm 14~V$ , it will be able to counteract  $\pm 700~mV$  of offset at the input. If a BJT input stage is being used with  $10\text{-}\mu\text{A}$  input bias current flowing through a  $50\text{-}k\Omega$  return resistor, offset at the input is -500~mV. The servo can handle this, but it will exhibit a constant output voltage of -10~V under quiescent conditions. This asymmetry will eat into the clipping headroom of the servo on low-frequency signals, leaving only 4~V on the negative side. This is an important consideration in the design of the servo.

#### The JFET Advantage

While some prefer JFET input pairs for reasons of sound quality and EMI resistance, there is another reason that makes them attractive. The JFET input stage does not suffer from DC offset caused by input bias current, and that makes the job of the DC servo much easier.

If an amplifier is to have reasonably high input impedance, its input return resistor must be large (at least  $20~k\Omega$ ). BJT input bias current flowing through this resistor will cause a far larger offset than the input voltage offset of the input pair or of input-referred offset from the VAS stage. If a JFET input stage is used instead, there is no DC offset from input

bias current, and the servo need only compensate for the 5-15 mV of offset of the JFET pair. The bottom line here is that the servo must typically work much harder when used in a typical DC servo arrangement with BJT input pairs as opposed to JFET input pairs.

### 8.3 The Servo Is in the Signal Path

The DC servo in Figure 8.5 is in the feedback path with modest gain at low frequencies. As such, the DC servo is in the signal path of the amplifier, and its performance can affect sound quality. The fact that it is injecting a signal at the input stage gives it opportunity to inject noise and distortion into the signal path. This can influence the quality of the audio signal, but is still better than having an electrolytic in the signal path.

For this reason, audio-grade op amps should be used for the DC servo's integrator and inverter. Pay attention to the noise and class B crossover distortion created by the op amp and consider pulling its output down to force its output stage to operate in class A. Design the servo as if it were part of a quality IC-based preamp. Provide a good clean power supply to the op amp and use a quality integrating capacitor (e.g., polypropylene film). The capacitor can be of slightly lower quality than those in the main signal path of the amplifier only because its output is attenuated before being applied to the input circuit.

#### **Servo Op Amp Distortion and Noise**

If the output of the servo is attenuated by 100:1 before application to the amplifier input and the amplifier has a closed-loop gain of 20, then the attenuation of the servo output to the output of the amplifier is only 5:1, or 14 dB.

There is thus flat gain (albeit usually less than unity) from the output of the servo to the output of the amplifier. This will depend on the ratio of the amplifier feedback resistor to the servo injection resistor. In some designs, this gain can be near unity. Given the fact that the output of the servo will be reproducing a strongly low-pass-filtered version of the output signal at some amplitude, it is possible for the servo op amp to create distortion that will make its way to the output of the amplifier. Indeed, if the servo op amp's output is hovering around zero, it could be experiencing some crossover distortion from the class B output stage of the op amp. This can be minimized by using a pull-down resistor on the output of the op amp to force its output stage into class A operation.

Noise created by the integrator and inverter op amps will be transported to the amplifier output with the gain mentioned above. The noise will also be influenced by the size of the integrator input resistor and the size of the integrator capacitor. Using a large input resistor, like 1 M $\Omega$ , allows the use of a much smaller integrator capacitor, sometimes as small as 0.1  $\mu$ F. This takes up less space and is less expensive to obtain in a high-quality capacitor. The price paid is increased servo noise. This noise increases at low frequencies, however, so its sonic effect is limited. It can be thought of as being akin to 1/f noise. If high impedances are used in the integrator, it is especially important to employ a JFET op amp for the integrator for two reasons. First, input base current of a bipolar op amp will create an undesirable DC offset voltage across the integrator input resistor. Second, the input noise current of a BJT op amp will cause significant noise with such a high-impedance source. The JFET op amp should be a low-noise design.

Beware of well-intentioned efforts to reduce servo noise and distortion. Some can result in instability, some can result in frequency response anomalies, and some can result in servo clipping. The very best way to reduce injected servo noise and distortion is to use high-quality parts and audio design practices in the servo.

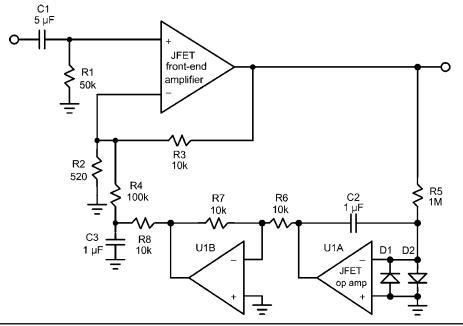


Figure 8.7 DC servo with additional low-pass filter.

#### **Adding a Second Pole**

The integrator in the DC servo may not be a perfect integrator at all frequencies. This can lead to some high-frequency program material or interference sneaking through the integrator. This leakage can be reduced by adding a passive low-pass filter at the output of the servo, as shown in Figure 8.7. This can be done by splitting the servo injection resistor and taking a capacitor from the junction to ground. This is implemented by R8 and C3, placing a pole at about 16 Hz. The idea is to further keep noise and distortion from the servo op amp out of the signal path. The DC servo of Figure 8.7 presumes the use of a JFET input stage in the amplifier and JFET op amps for the DC servo.

However, this technique can have subtle effects on the low-frequency response if it is not implemented with care. This is because the frequency-dependent impedance seen looking back into the servo injection network acts as though it is in parallel with the main negative feedback network shunt resistor to ground (R2). The low-frequency response step created in the design of Figure 8.7 is only 0.005 dB. The added capacitor is also somewhat in the effective signal path, so its quality matters.

A different approach is shown in Figure 8.8. It can be implemented in the case of a servo with an inverting integrator followed by an inverter, as in Figure 8.5. Some capacitance can be put across the inverter's feedback resistor, giving the inverter a low-pass response. Here the second pole is implemented by C3 working against R7, producing a pole at 16 Hz. This approach still leaves the door open a crack for noise and high-frequency sneak-through from the inverter, however.

Adding a second pole to a feedback loop usually invites instability or frequency response peaking if it is not done carefully. Figure 8.9 shows the frequency response of a poorly designed servo. In order to avoid this, the added pole should be well above the

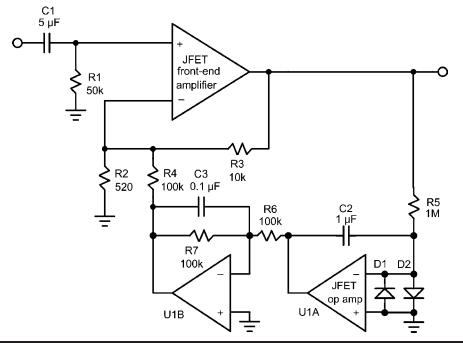


FIGURE 8.8 DC servo with LPF implemented with a capacitor around the inverter.

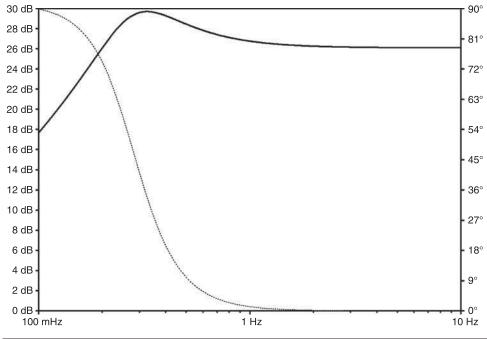


FIGURE 8.9 Frequency response of a poorly designed DC servo.

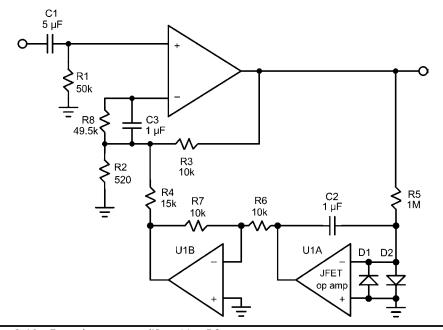
servo bandwidth frequency, perhaps by a decade. This constraint is easily satisfied in both of the designs above where the servo bandwidth is only 0.016 Hz.

### 8.4 DC Offset Detection and Protection

The servo's integrator output provides a convenient monitoring point for the DC health of the amplifier. If DC persists at a certain voltage level over a certain period of time, the servo integrator will build up a large voltage to try to counteract the DC offset. This voltage can be fed to a window detector to open the speaker relay or otherwise engage protection circuits. The window detector can be constructed from two comparators, each fed an appropriate threshold voltage. If there is a known typical servo offset due to the use of a BJT input pair, then the servo output should be offset before application to a symmetrical window detector, or the window edges will have to be made asymmetrical. There will be some error in this approach, since the BJT base currents that cause the offset may be different for each amplifier and are temperature dependent. Once again, JFETs are at an advantage, but keep in mind that a JFET offset of 10~mV will create 2~V of servo output offset uncertainty in the design shown having a  $100\text{-k}\Omega$  servo injection resistor. The difficult trade-off of servo injection resistor size, relative to the feedback resistor, is once again highlighted.

# 8.5 DC Servo Example

The amplifier shown in Figure 8.10 has a closed loop gain equal to 20, set with a 10-k $\Omega$  feedback resistor and a 520- $\Omega$  feedback shunt. The DC servo uses an inverting servo integrator with a 1-M $\Omega$  series resistor and a 1- $\mu$ F capacitor. The integrator will have a gain of 0.16 at 1 Hz.



**FIGURE 8.10** Example power amplifier with a DC servo.

Assume a unity-gain servo inverter at the output of the integrator. A 15-k $\Omega$  servo injection resistor connects the servo inverter to the inverting input of the power amplifier, providing a servo attenuation factor of about 30:1. The servo loop gain at 1 Hz will be the integrator gain times the ratio of R3 to R4. This equals 0.11. This means that the low-frequency cutoff created by the servo is at about 0.11 Hz (the servo-based LF cutoff is simply the frequency where the servo loop gain falls to unity).

We have an LF cutoff frequency of only 0.11 Hz, not simply because we wanted to really go low, but because the numbers will work out nicely, especially in terms of servo signal-handling ability. Bear in mind that the overall amplifier low-frequency cut-off will still be largely determined by the input coupling capacitor.

With a 30:1 servo attenuation factor and op amps capable of  $\pm 14$  V, servo correction range is only  $\pm 470$  mV. The BJT input stage requiring 10  $\mu A$  combined with a 50-k $\Omega$  return resistor requires more than that. Moreover, at that point all of the servo's dynamic range for handling AC feedback signals at low frequencies is used up. This servo requires the use of high- $\beta$  BJTs or JFETs at the input. The optional DC balance network consisting of R8 and C3 can be added to reduce the effects of BJT input offset current.

Assume that this is a 100-W amplifier with a 40-V peak output. Let the DC protection be triggered when the servo output reaches a threshold of 6 V. If the servo needs to correct a fairly large input offset of 100 mV, the servo output only goes to about 3 V, well within its safe range. The servo can handle nearly 200 mV offset before triggering DC protection and is still not even close to the output limits of the integrator op amp. However, LF signal swings have yet to be taken into account.

With a full-power (40-V peak) 10-Hz sinusoid produced by the amplifier, the sinusoidal output of the servo integrator will only be about 0.6-V peak. It will be 10 times this if the input signal is at 1 Hz and will just trigger the DC protection (in the absence of offset correction). If the amplifier fails shorted to a rail and produces 40 V of DC, the servo integrator output will rise to the 6-V protection trigger point within 0.25 second.

If we want to reduce servo influence at the expense of offset that can be handled, we can simply increase the servo injection resistance from 15 to  $50~\mathrm{k}\Omega$ . This will reduce by 10 dB the opportunity for servo noise and distortion to get into the signal path. This will also reduce the LF cutoff to 0.03 Hz. As long as the amplifier design and architecture does not cause a turn-on settling issue that must be corrected, there is probably no problem with this lower LF cutoff frequency. The peak voltage at the output of the integrator will increase by nearly a factor of 3 for a given amount of offset correction. This may increase the chances of triggering DC protection circuits. This approach is best suited to a JFET input LTP so that base current offsets are absent.

If for some reason we want to go to a higher LF cutoff frequency, we must increase servo loop gain. We can do this by reducing the  $15\text{-k}\Omega$  servo injection resistance at the expense of greater opportunity for servo garbage to get into the signal path. Alternatively, we can achieve the same result by increasing the integrator gain. Changing to a  $0.1\text{-}\mu\text{F}$  integrator capacitor will increase the integrator gain by a factor of 10 and bring the LF cutoff up to 1 Hz. Unfortunately, the servo is now more easily overloaded by large low-frequency signals at the amplifier output. A full-amplitude 10-Hz signal at the output of the amplifier will now cause triggering of the DC protection. This is just a design decision and it may be OK. Many audiophiles would not want a high-level signal at 10 Hz to drive their loudspeakers anyway.

There are many possible variations to this kind of servo, but this is a good illustration of typical operation and trade-offs.

## 8.6 Eliminating the Input Coupling Capacitor

A system signal path often contains more coupling capacitors than necessary. There will usually be one at the output of the preamplifier, and yet another one at the input of the power amplifier. If the power amplifier has a DC servo, the input coupling capacitor of the amplifier can be bypassed, knowing that the output of the preamp is probably at or very close to zero. This is no more risky than using a DC-coupled power amplifier. Any small DC offset present at the input of the amplifier will be handled by the DC servo. In this case, an overall improvement in low-frequency transient response will have been had by the use of a servo. Removal of the input coupling capacitor is strictly a choice in regard to managing risk. Many DC-coupled power amplifiers have the option of switching in a blocking capacitor at the input. This is a good idea that can be applied in the general case if one uses a servo in the power amplifier.

## 8.7 DC Servo Design Issues and Nuances

It is easy even for experienced designers to fall into a trap when it comes to servo design. Just because the servo may not need to do much correction in some designs, do not make the mistake of making the servo strength too small. If you do, the integrator gain will be necessarily higher, all else remaining equal, and the servo will be vulnerable to clipping on large subsonic signals.

### **Servo Start-Up Transients**

The servo will often be designed to have a very low-frequency cutoff. This reflects the fact that it should act largely as a long-term automatic screwdriver adjustment. The integrator capacitor will start out at zero on power-up, so initially there will be no servo correction. This means that the power-on transient will include the uncorrected offset of the amplifier, which will often be dominated by the offset induced by base current in the case of a BJT input stage. A power-on delay implemented with a speaker relay will eliminate this.

#### **Low-Frequency Testing of Amplifiers Employing Servos**

Full-power testing of power amplifiers at frequencies well below 20 Hz may cause problems with servo clipping or with servo-based DC protection. This is because the servo is merely an integrator fed with the output signal of the amplifier. The integrator gain increases as frequency decreases. Consider an amplifier producing 45 V peak at its output. At a frequency where the integrator gain has risen to 1/3, the signal at the output of the integrator will be 15 V peak, enough to clip the integrator op amp.

#### **Simulation**

It is wise to conduct a SPICE simulation of all DC servo designs to verify behavior. This is especially the case when verifying the LF amplifier corner and any frequency response peaking that might occur. This can be done with an AC simulation.

The issue of unbalanced LTP return resistances and resulting need for correcting servo action can be evaluated with a DC simulation. Static offset at the output of the servo should always be evaluated.

